National Institute of Technology

Rourkela

ATLAS SIMULATION BASED STUDY OF SOI TUNNEL FET

A thesis submitted in partial fulfillment of the requirements for the degree of Bachelor of Technology in Electronics and Instrumentation Engineering

BY:

SAROJ KUMAR
110EI0430

KHIROD KUMAR MAJHI
110EI0241

Under supervision of:

Prof. Pramod KumarTiwari

Department of Electronics & Communication Engineering
NATIONAL INSTITUTE OF TECHNOLOGY, ROURKELA
ODISHA, INDIA – 769008

CERTIFICATE

This is to certify that the Thesis entitled "ATLAS SIMULATION BASED STUDY OF SOI TUNNEL FET" submitted to the National Institute of Technology, by Mr. Saroj Kumar, Roll No.-110EI0430 And Mr. Khirod Kumar Majhi, Roll No.-110EI0241 for the award of the degree of Bachelor of Technology In Electronics And Instrumentation Engineering, is a bonafide record of research work carried out by them under my supervision and guidance.

The Candidates have fulfilled all the prescribed requirements.

The thesis, which is based on candidate's own work, has not been submitted elsewhere for a degree/diploma.

In my opinion , the thesis is of standard required for the award of a Bachelor of Technology degree in Electronics and Instrumentation Engineering.

To the best of my knowledge, they bear extremely good moral character and decent behavior.

Prof. P.K.Tiwari

Department of Electronics and Communication Engineering

National Institute of Technology

Rourkela (INDIA-769008)

ACKOWLEDGEMENT:

We are extremely grateful towards Prof. Pramod Kumar Tiwari for his priceless advice and instructions. We would also like to extent our hearty gratitude towards Mr. Gobi Krishna , P.H.D scholar for their extended support and assistance in completing this paper.

TABLE OF CONTENTS PAGE NO.

ABSTRACT

We observed that there are two limitation with conventional Mosfet, especially Sub-threshold swings .Its minimum value is 60mv/decade. But we cannot get less sub-threshold swing with conventional Mosfet.
In order to decrease Sub-threshold further , we use tunnel FET's to reduce swing to some-what less value than conventional mosfet .Tunnel- fet is working on tunneling effect , which require less input voltages to decrease band gap due to presence of p-i-n region . There are also very low OFF- current in tunnel – FET. In tunnel–fet there is low power consumption.
The TFET works on band-to-band tunneling (BTBT)principle , which will be studied .

CHAPTER-1 INTRODUCTION

At initial stage of Mosfet which is invented and patented by Lilienfeld and heil in the year 1930, but it was successfully demonstrated in 1960. At initial stage of invention there were lots technological problem. These problems especially associated with control and reduction of the surface area interface between semiconductor and the oxide layer. Initially, only "**depletion-mode**" was available, initially which required negative voltage to the gate to deplete an existing n-type channel. In depletion-mode device having a conducting channel between source and drain without applying any gate voltages. Fabrication of new device by applying reduction in surface area, which enabled us to fabricate a device which do not have initial conducting channel between source and drain. Such devices are referred to as "**enhancement-mode**" devices. In this devices the electrons at oxide-semiconductor are concentrated in a thin (~10 nm thick) "inversion layer". Now a day, we mostly use enhancement –mode devices.

MOSFET stands for metal oxide field's effect transistor, which act as a voltage- controlled current device. It is a device in which current at two probes i.e source and drain is controlled by action of electric field at another probe gate having in – between semiconductor and metal very a thin metal oxide layer. MOSFETS mainly encompasses of four parts namely source(S) , gate(G) , drain(D), and body(B) terminals. The body is connected with source terminals, making it a three- terminal device. Since these two normally connected to each other, making it a three- terminal device.

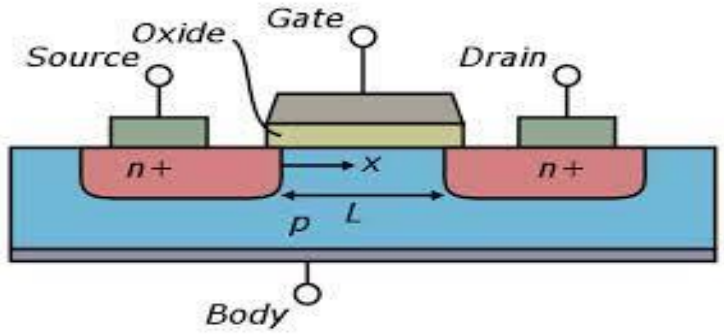


FIGURE 1.1[1]

TWO COMPLEMENTARY DEVICES :-

- n- channel devices (n-MOSFET) on p-Si Substrate
- P- channel devices (p-MOSFET) on n-Si Substrate

1.1 TYPES OF MODES IN A MOSFET

In enhancement mode MOSFETs , voltage applied across the gate and hence it creates a conducting channel between the source and drain contact via the field effect . As term "enhancement" define before , its name already give us a idea of something to enhance …that mean in during channel creation , it enhance the conductivity with increase of gate voltages , which adds more no. of electrons to channel , it also referred to as the *inversion layer* . There are two types of channel, one channel which contain electrons known as nMOSFET or nMOS and one channel which contains hole is known as pMOSFET or pMOS. But with substrate it totally opposite in type so, nMOS is made with a p-type substrate, and pMOS with an n-type substrate.

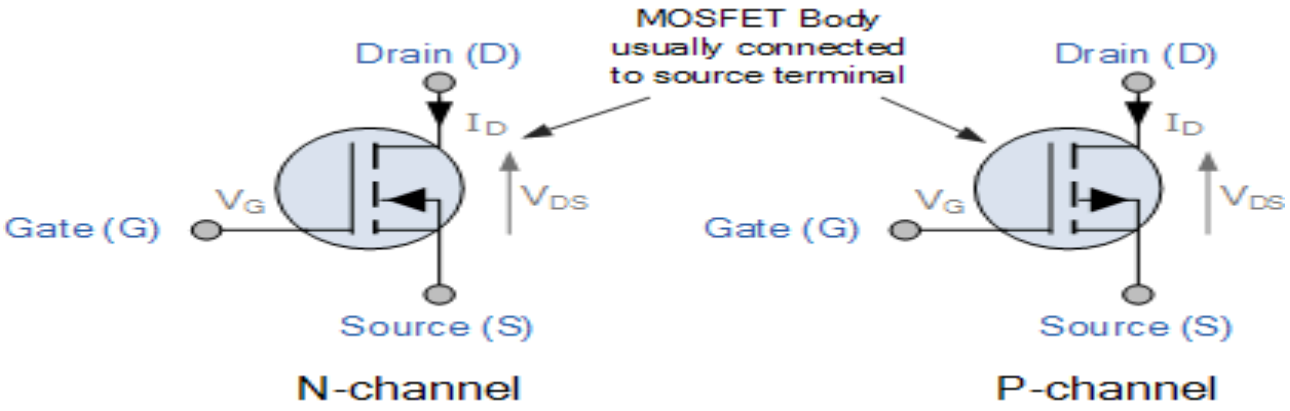


FIGURE -1.1.2[2]

FIGURE-1.1.3[3]

With voltage across Vgs = 0 V, then there is creation very thin channel, as we increases the gate voltages, the channel width gets enhances .

There are pair of n-region across drain and source electrode. As we increase the gate voltages, the large no. of hole pull to p-type substrate and electrons push towards n- region under the drain and source electrode. As we increase the gate voltages the channel width gets more thick . so , there is large flow of current from drain to source under electric field created by metal oxide and semiconductor layer. **[1]**

1.2 THREE OPERATIONAL MODES:-

1 .Cut-off mode:

- There are some condition to operate in cut-off reason:
- Vgs < Vt , Vgd < Vt with Vds> 0. Where Vt threshold voltages of the devices . In , this condition there is no current between drain and source Id = 0 , because according to threshold model , the transistor is in off condition.

2. Linear or triode regime:

- Condition for triode regime :-
  Vgs > Vt , Vgd > Vt and Vgd >0
  In this reason transistor is in ON mode .During ON mode ,there is formation of thick layer of channel . Due to this channel there is flow of current between drain and source. MOsfet work like a resistor , and it is totally controlled by gate voltages relative to both the source and drain voltages . The drain current between drain and source electrode is **[2]**

$$I_D = \mu_n C_{ox} \frac{W}{L} \left((V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

Where **W** is the gate width , **L** is the gate length and Cox is the gate oxide capacitance per unit area .

3.Saturation mode

- Condition for Transistor to operate in Saturation mode:-
- VGS > VT (induced channel)
- , VGD < VT (pinched – off channel)
- (VDS > 0)

In this mode ID is independent of VDS .

In saturation region , the drain voltages is more than that of gate voltages . The saturated MOSFET behave as an ideal current source whose value is controlled by gate voltage .According to the non-relationship in below equation :-

$$i_D = \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - V_t)^2$$

This is equation based on some assumption ..But if we further increase the drain voltages ,this voltages drop across the narrow depletion region between the end of the channel and the drain region . This voltages accelerate across the electrons that reach the drain end of channel and sweeps them across the depletion region into the drain. However ,the channel length is in

effect reduced. This show the weak dependent on drain voltages and controlled primarily by the gate- source voltages, and modeled approximately as:

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{th})^2\,(1 + \lambda(V_{DS} - V_{DSsat}))\,.$$

The additional factor invoving lamda , is a channel length moudulation parameter , this equation shows that there is drain current depend on drain voltages .

`

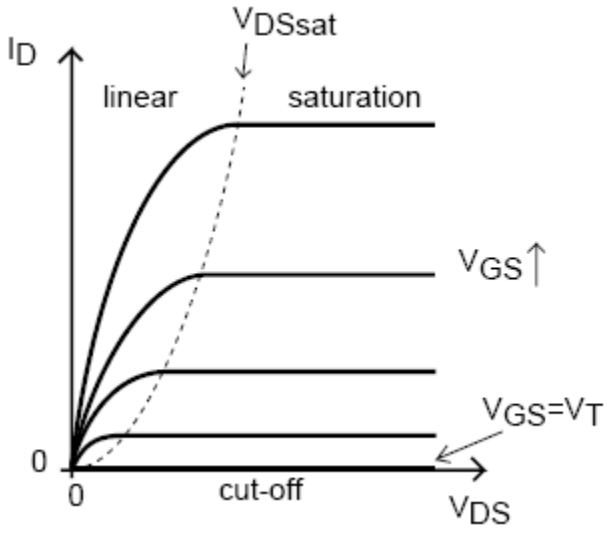


FIGURE 1.2[4]

- KEY DEPENDENCIES:-
- VDS increases ---------- Id increases(higher electric field)
- Vgs increases ----------Id increases(higher electron conc.)
- L increases ---------- Id decreases(lower lateral electric field)
- W increases ----------Id increases (wider conduction band)

1.3 DISADVANTAGES FACED BY CONVENTIONAL MOSFET:

There are many limitation faced by conventional MOSFET . A theory coined by Robert H. Dennard proposed a scaling theorem, according to which electric field remain constant throughout . According to that we decreased VDD by 20% , VT decreased by its half value , this actually did not happen with conventional MOSFET , when we decreased VDD by some value but VT decreased significantly very less. Due to which gate overdrive decreased significantly, because of that ON- current decreases and dynamic speed deceased which affect the device performance.
There are two possible solution to eliminate this problem with conventional MOSFET.

1- Either VDD can stay higher than it should wiyh constant field scaling or,
2- VT can be scaled down more aggressively

In order to maintain the level of gate overdrive value, VDD has slow down drastically .When VDD did not decreased significantly ,then there lots of power loss

$$P_{Dynamic} = FCLV_{DD}pow(2)$$

Where f is frequency and CL is total switched capacitive load

$$P_{static} = I_{leak} V_{DD}$$

Where l leak is sum of leakage currents in device when the MOSFET is in the off-state.

The main disadvantage of conventional Mosfet is :-
1-It has high power consumption
2-It has threshold swing around 60 mv/decade .we cannot reduced further in case conventional MOSFET.

1.4. THRESHOLD- SWING :-

It is feature of MOSFET's current – voltage characteristic .It is defined as the change in gate voltage required to change the drain current by one decade**.[4]**

$$S = \frac{dV_g}{d(\log I_d)} [\text{mV/dec}]. \qquad (1)$$

Where Vg is the gate voltage and Id is the drain current.

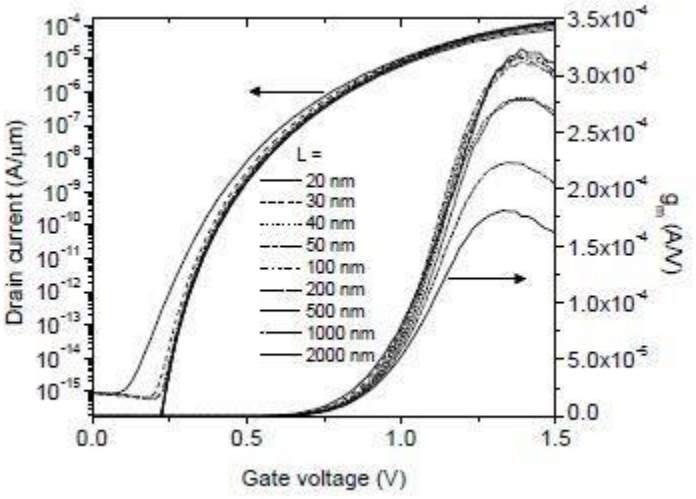


FIGURE 1.4[5]

1.5-**TUNNEL FET**

1.5.1 INTRODUCTION:-

Tunnel FETs also referred as TFETs or Tunneling FETs , for replacement of conventional MOSFETs . It can be used for low power consumption application. It also offer very low threshold swing .It is used for low power consumption because ,it has very high OFF-current .Other things which help for low power consumption ,because of their quantum tunneling barrier. When the device turn On , the carrier must have to tunnel through barrier for current to flow between drain and source. When this devices turn off it posses very large barrier for carriers ,which does not an carrier to flow this barrier .Because of that there is no current floe between drain and source.It made very low OFF- current(approx.-e-17A).Which is very less than conventional MOSFET.

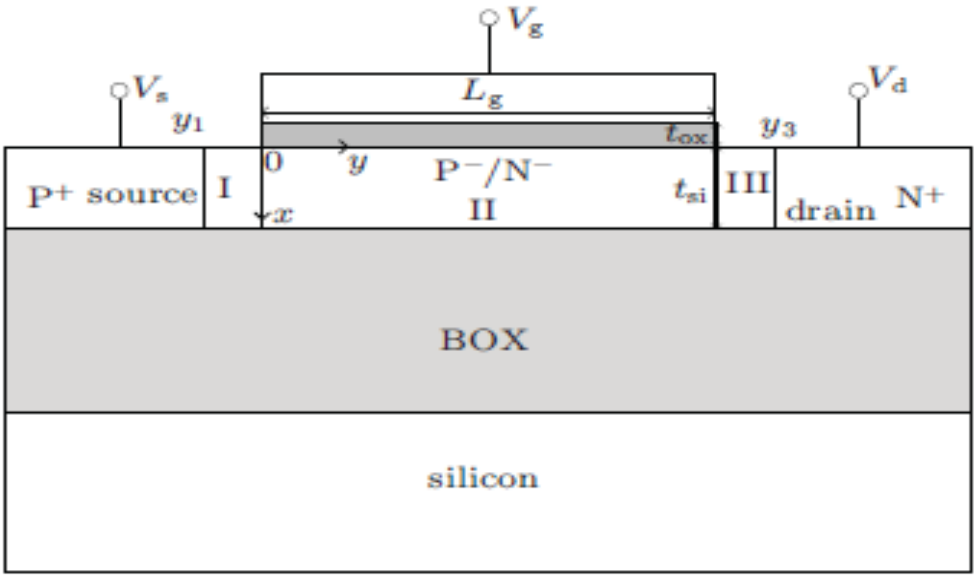


FIGURE 1.5.1[6]

1.5.2 Structure and its operation:

Tunnel fets are gated p-i-n diodes . To operate it ,first we have to apply reversed biased across drain and source and a voltage is applied at gate. Reversed bias is used across p-i-n diodes to create tunneling . Now , there are two types of TFETs-one NMOS ,in which n is drain and p is source and +ve voltage is applied across gate. Other TEFTs is PMOS , in p+ is drain and n_ is source and –ve voltage us applied at gate. When –ve gate voltage is applied to gate . The energy bands in the intrinsic under the gate are lifted and energy barrier close enough for band to band tunneling between valence band of intrinsic region and conduction band of n+ region. When +ve voltage is applied at gate , then intrinsic region are pushed down and tunneling take between valence band of p+ region and conduction band of intrinsic region**.[3]**

The energy barrier's width between the intrinsic region and p+ regions is played a vital role in ON-current of TUNNEL-FETs, the current depend exponentially on barrier width. The barrier width start to saturate at high Vgs.

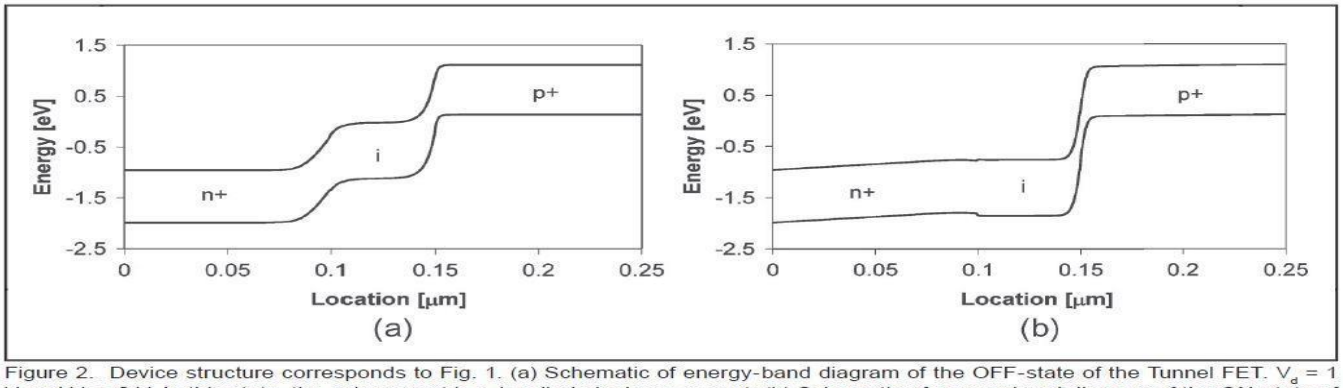


Figure 2. Device structure corresponds to Fig. 1. (a) Schematic of energy-band diagram of the OFF-state of the Tunnel FET. V_d = 1 V and V_g = 0 V. In this state, the only current is p-i-n diode leakage current. (b) Schematic of energy-band diagram of the ON-state of the Tunnel FET. In this state, the energy barrier is thin enough that electrons can tunnel from the valance band of the p+ region to the conduction band of the intrinsic region. V_d = 1 V and V_g = 1.8 V.

FIGURE 1.5.2[7]

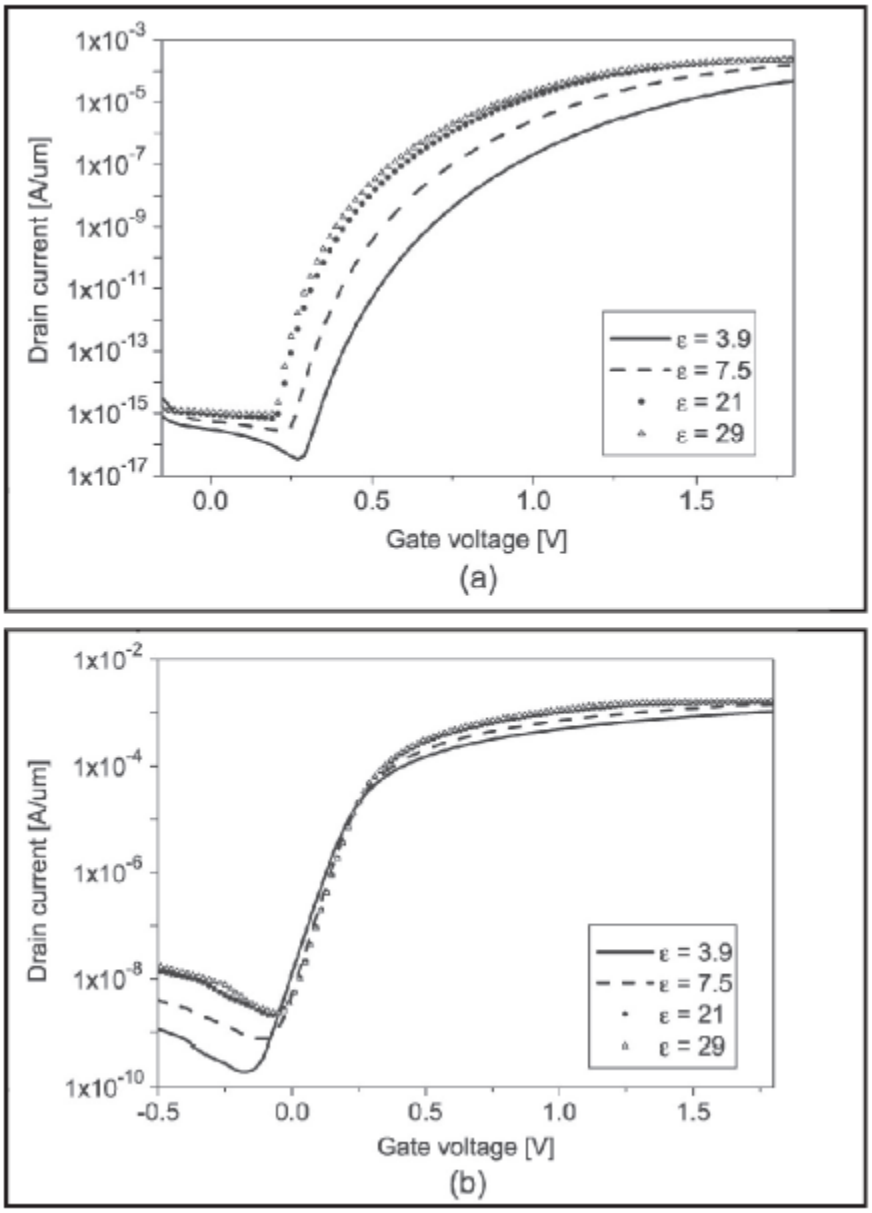


figure 1.5.3[8]
TRANFER CHARCTERISTICS TO VARIOUS DIELECTRICS

CHAPTER 2. SIMULATION USING ATLAS

All 3-D programs in ATLAS supports structures made public on 3D prismatic meshes. Structures might have absolute geometries in two dimensions and include multiple slices at intervals the dimension .There area unit two ways in which for creating a 3D structure which is able to be used with ATLAS. a method is through the command syntax of ATLAS, in our own means is through associate degree interface to DEVEDIT3D. [5]

Mesh generation

Normally, slices are created perpendicular to the Z axis. The mesh is triangular in XY however Rectangular in XZ or YZ planes.

Region,Electrode, and Doping definition

To Define a Structure" also covers the definition of 2D regions, electrodes and doping profiles. To extend the regions into 3D, use the Z.MIN and Z.MAX parameters. For example:

```
REGION NUM=2 MATERIAL=Silicon X.MIN=0 X.MAX=1 Y.MIN=0 Y.MAX=1 Z.MIN=0 Z.MAX=1
ELECTRODE NAME=gate X.MIN=0 X.MAX=1 Y.MIN=0 Y.MAX=1 Z.MIN=0 Z.MAX=1
DOPING GAUSS N.TYPE CONC=1E20 JUNC=0.2 Z.MIN=0.0 Z.MAX=1.0
```

For 2D regions or electrodes defined with the command language, geometry is limited to rectangular shapes. Similarly, in 3D regions and electrodes are composed of rectangular parallelepipeds.

The models available are

MOBILITY

Thomas (ANALYTIC)

Table for 300K (CONMOB)

Arora's Model (ARORA)

Lombardi's Model (CVT)

Yamaguchi Model (YAMA)

Parallel Field Dependence (FLDMOB)

Recombination

Shockley Read Hall (SRH)
Concentration dependent lifetime SRH (CONSRH)
Klaassen's concentration dependent lifetime SRH (KLASRH)
Optical Recombination (OPTR)
Auger (AUGER)
Bulk and interface traps (TRAP, INTTRAP)
Continuous defect states (DEFECT)

Generation

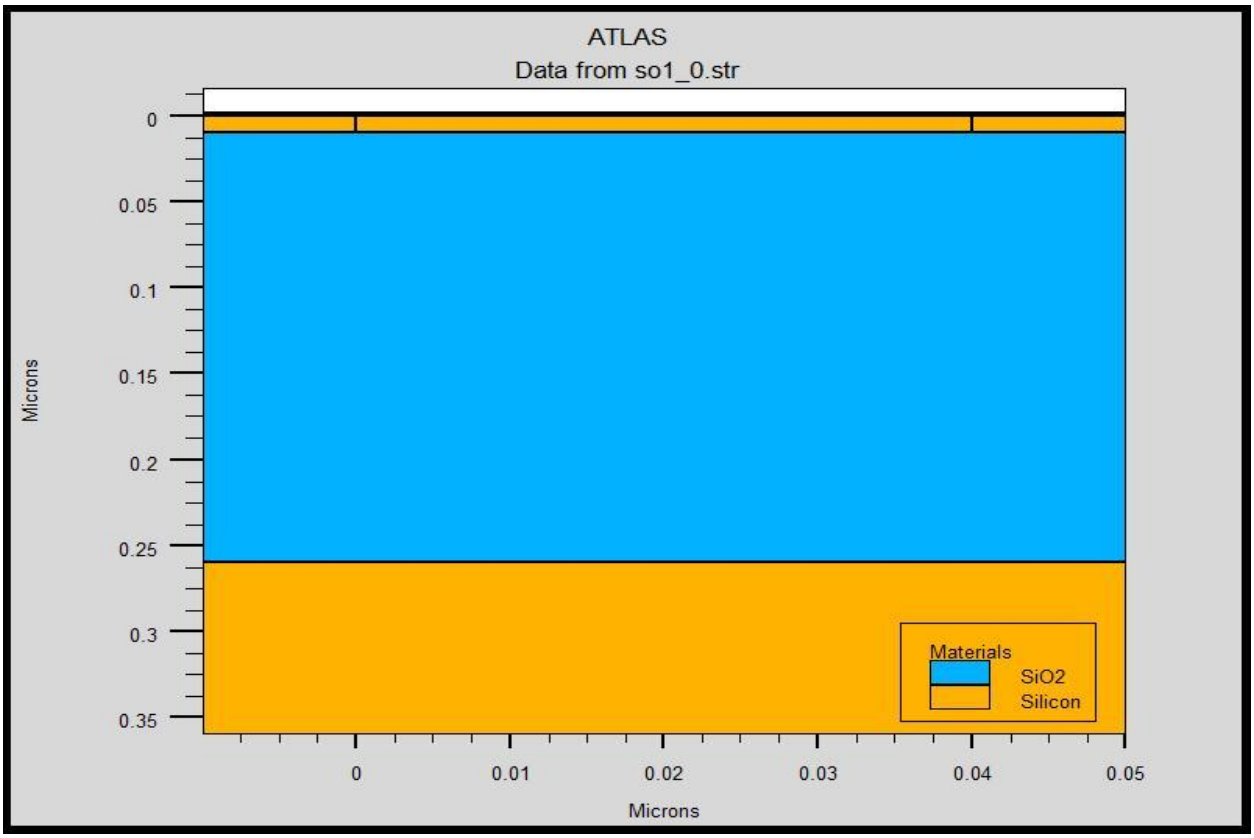
Crowell Impact Ionization (IMPACT CROWELL)
Hot Electron Injection (HEI)
Single Event Upset (SINGLEEVENTUPSET)

Carrier Statistics

Boltzmann (default)
Quantum Mechanical Effects (QUANTUM)
Band Gap Narrowing (BGN)
Incomplete Ionization (INCOMPLETE)
Fermi (FERMI)

CHAPTER 3: RESULTS AND DISCUSSIONS

DESIGN 1 : SIMULATED STRUCTURE OF TUNNEL-FET FOR CHECKING ENERGY BAND-LEVELS



Region 1-silicon dioxide layer has length of 2nm at the top of source, drain and gate
Region 2-gate region has length of length of 40 nm and width of 10 nm
Region 3- buried oxide or sio2 layer of has length of 60nm and width of 250nm
Region 4-substrate of si below insulator of has length of 60nm and width of 100nm
Region 5-source region has length of 10 nm and width of 10nm
Region 6-drain region has length of 10nm and width of 10 nm
Hence by dividing into specific regions, the structure was designed adequately. The box region is made up of sio2.and substrate is made up of silicon.
The doping concentration in region2---uniform, p-type $2x10^{17}$

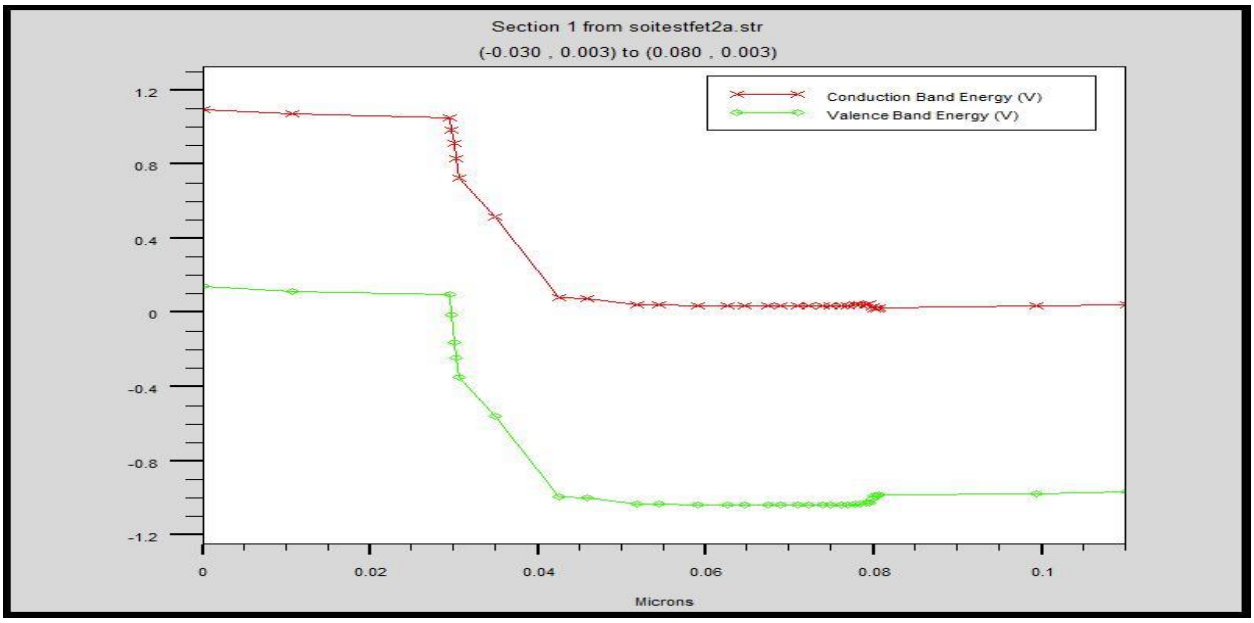
The doping concentration in region3---uniform, p-type $2x10^{17}$

The doping concentration in region5---uniform, n-type 10^{20}

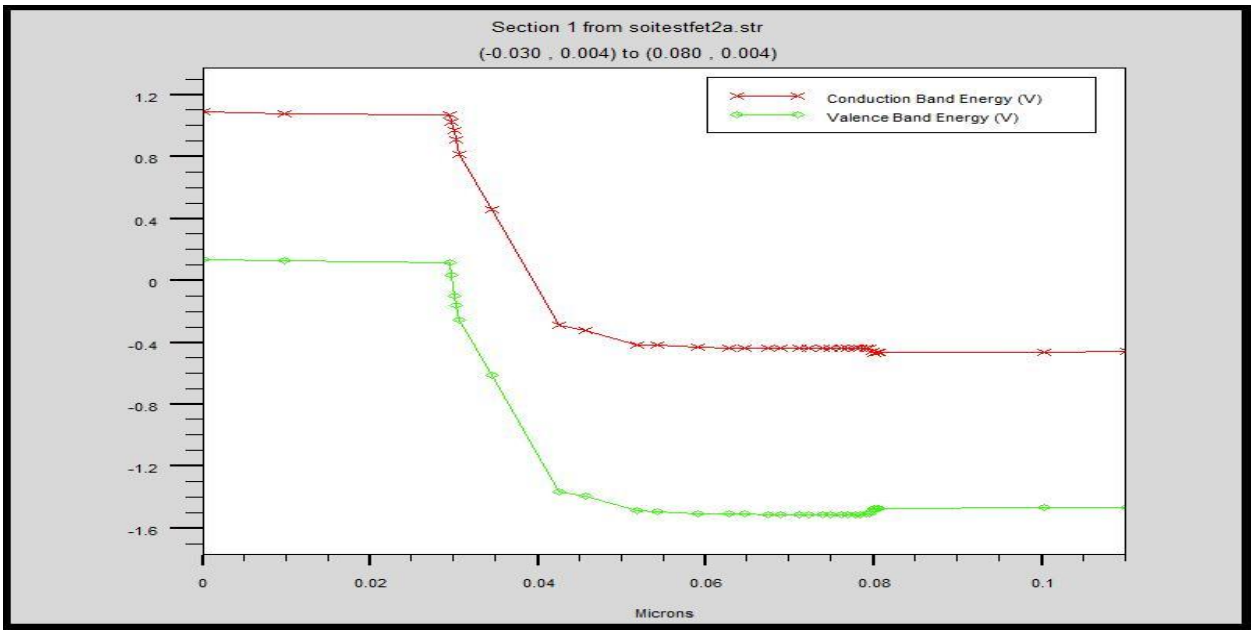
The doping concentration in region6---uniform, n-type 10^{20}

BAND ENERGY DIAGRAMS FOR DIFFERENT VALUES OF Vds

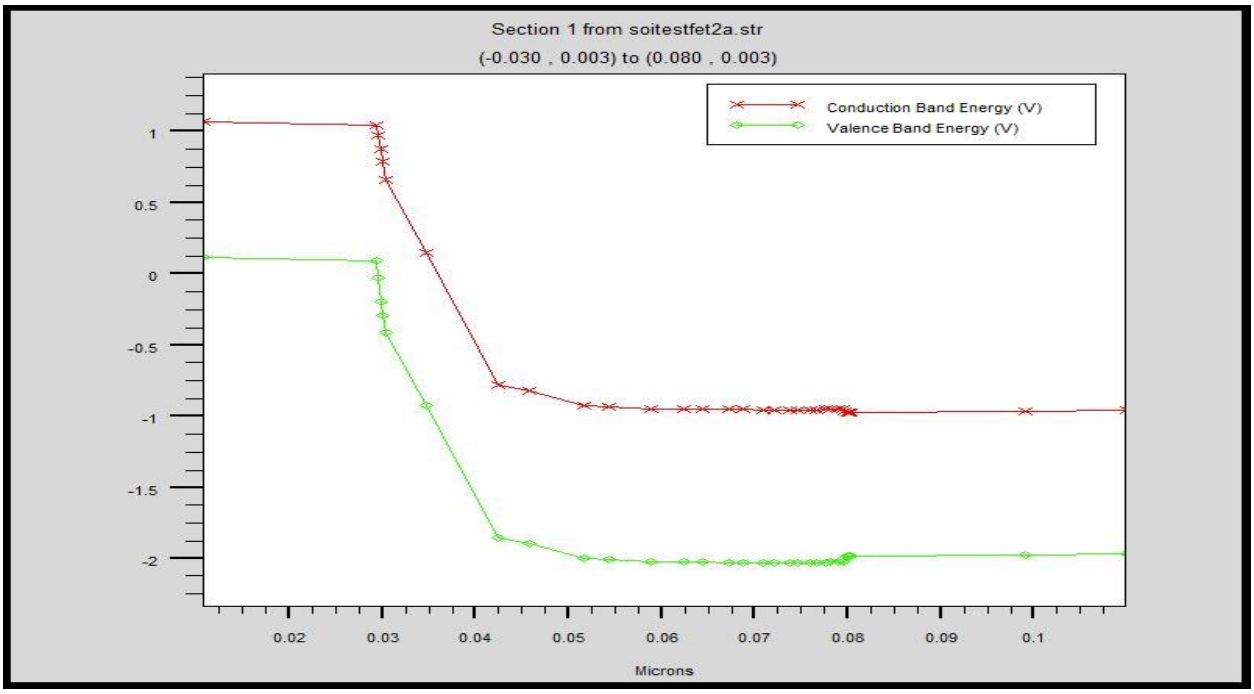
(A) Vds = 0 V



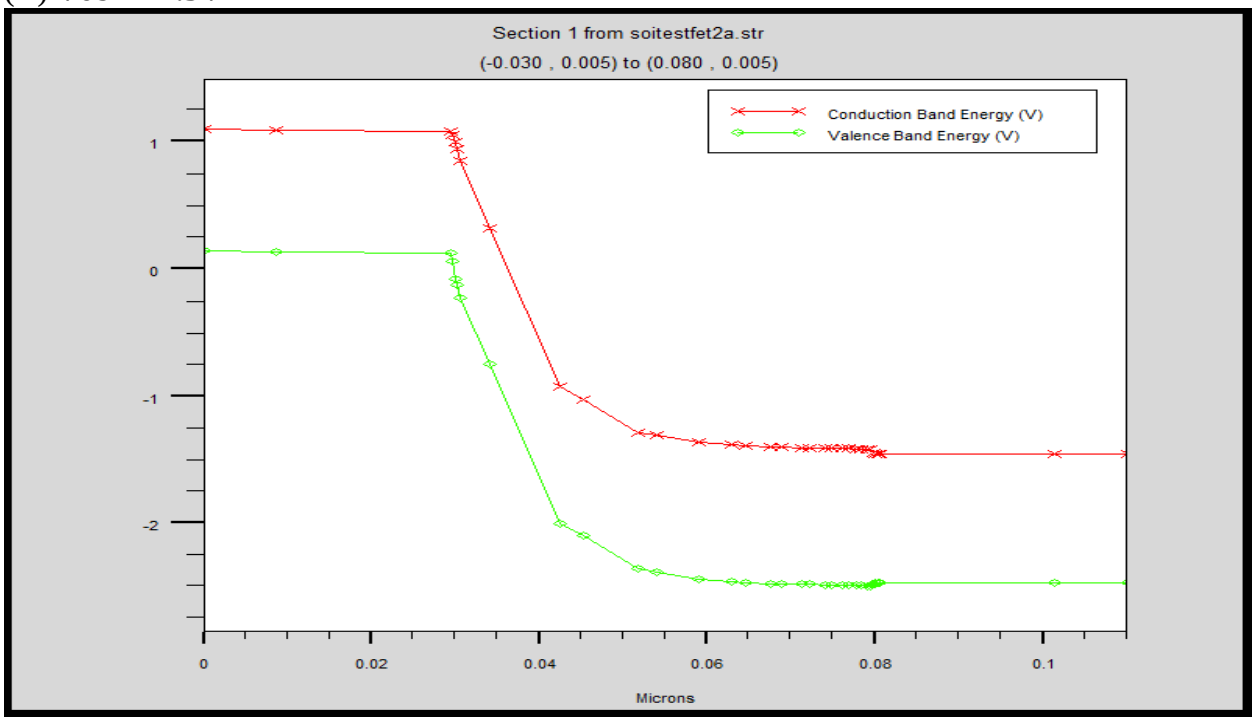
(B)**Vds = 0.5V**



(C)**Vds = 1 V**



(D) **Vds = 1.5V**

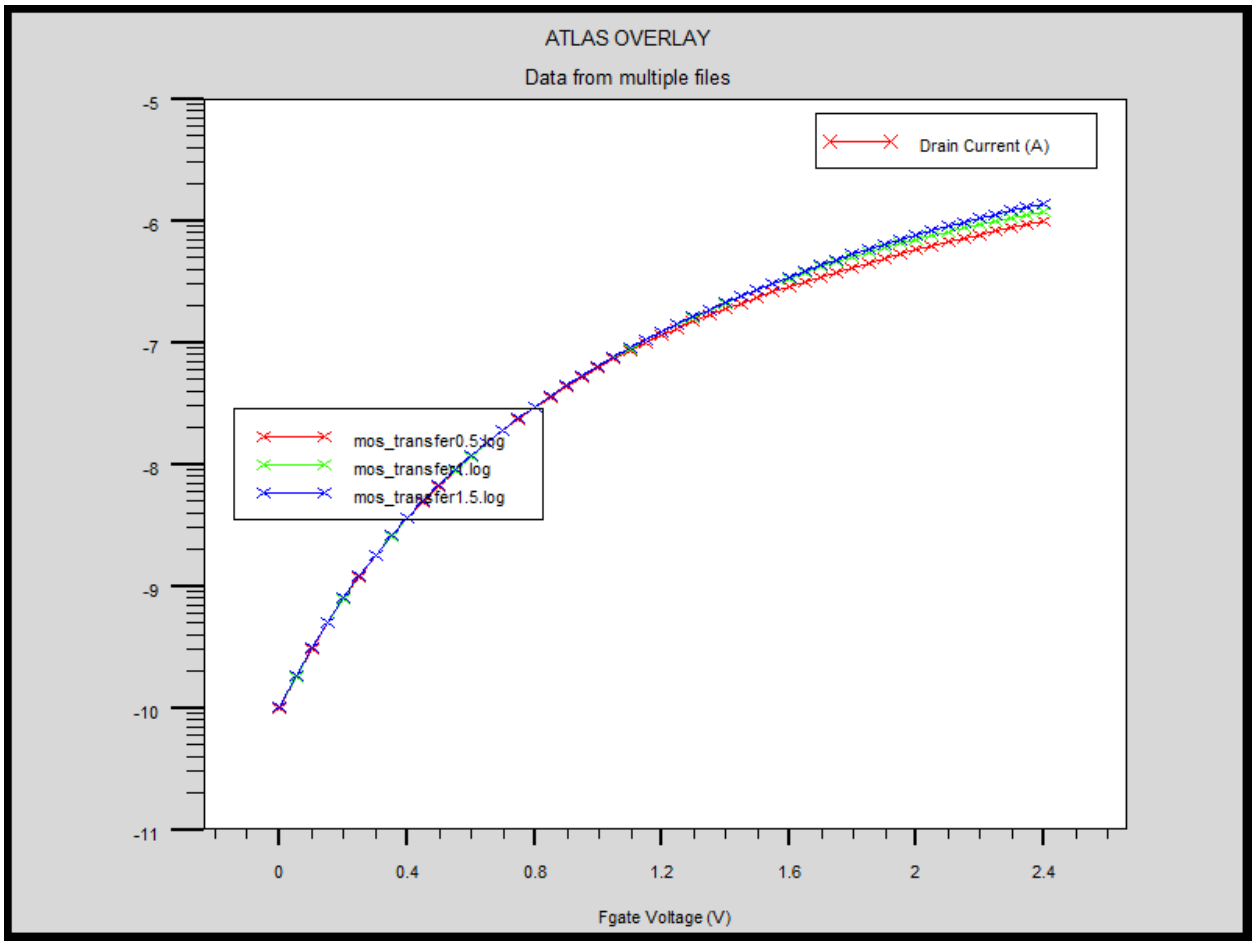


ANALYSIS :

It can be seen that by as the gate voltage is increased , the conduction band and the valence

band converge more , thus allowing the tunnel effect to take place easily.

TRANSFER CHARACTERISTICS



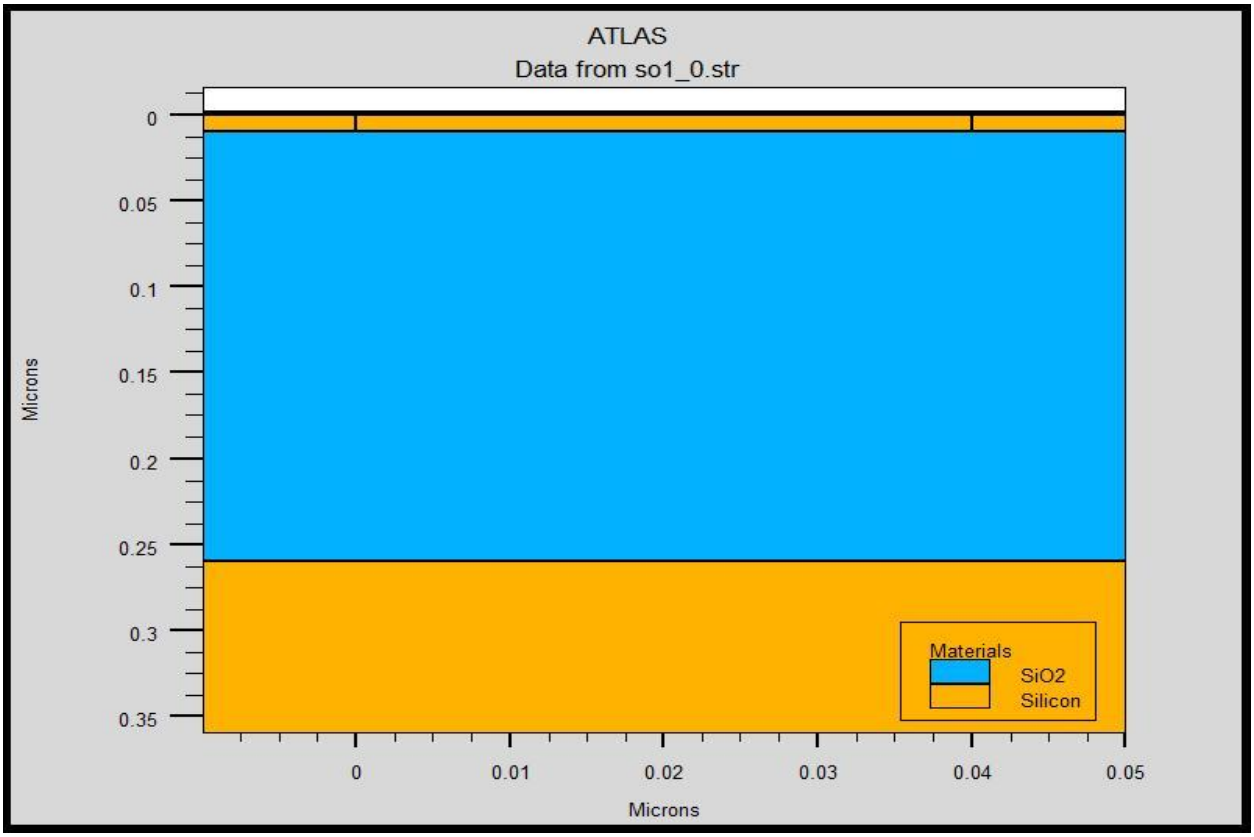
ANALYSIS:

The curve between drain current vs gate voltage was plotted by taking a constant vds=0.5v.Different values of drain currents were obtained for different values of gate bias voltage. So the above characteristics were obtained as shown in the above curve.

It can be seen that current is nearly same when gate voltage is less , but as gate voltage increases the curve of the fet with more drain voltage increases more than the others.

.

DESIGN 2 : SIMULATED STRUCTURE OF TUNNEL FET FOR ANALYSING OFF-CURRENTS



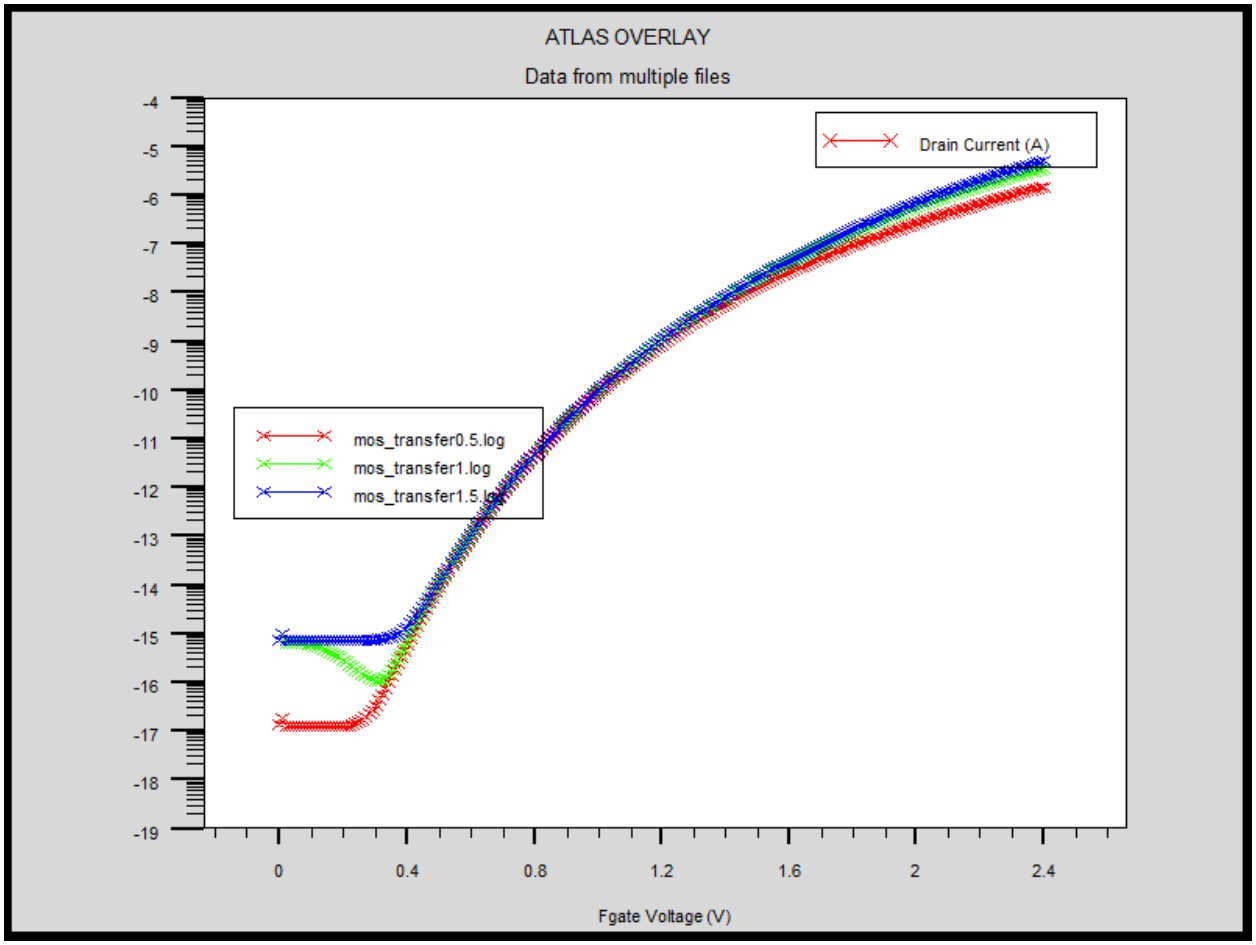
Region 1-silicon dioxide layer has length of 2nm at the top of source, drain and gate
Region 2-gate region has length of length of 40 nm and width of 10 nm
Region 3- buried oxide or sio2 layer of has length of 60nm and width of 250nm
Region 4-substrate of si below insulator of has length of 60nm and width of 100nm
Region 5-source region has length of 10 nm and width of 10nm
Region 6-drain region has length of 10nm and width of 10 nm
Hence by dividing into specific regions, the structure was designed adequately. The box region is made up of sio2.and substrate is made up of silicon.
The doping concentration in region2---uniform, p-type $2x10^{17}$

The doping concentration in region3---uniform, p-type $2x10^{17}$

The doping concentration in region5---uniform, n-type 10^{20}

The doping concentration in region6---uniform, n-type 10^{20}

TRANSFER CHARACTERISTICS (Id vs Vgs curve)



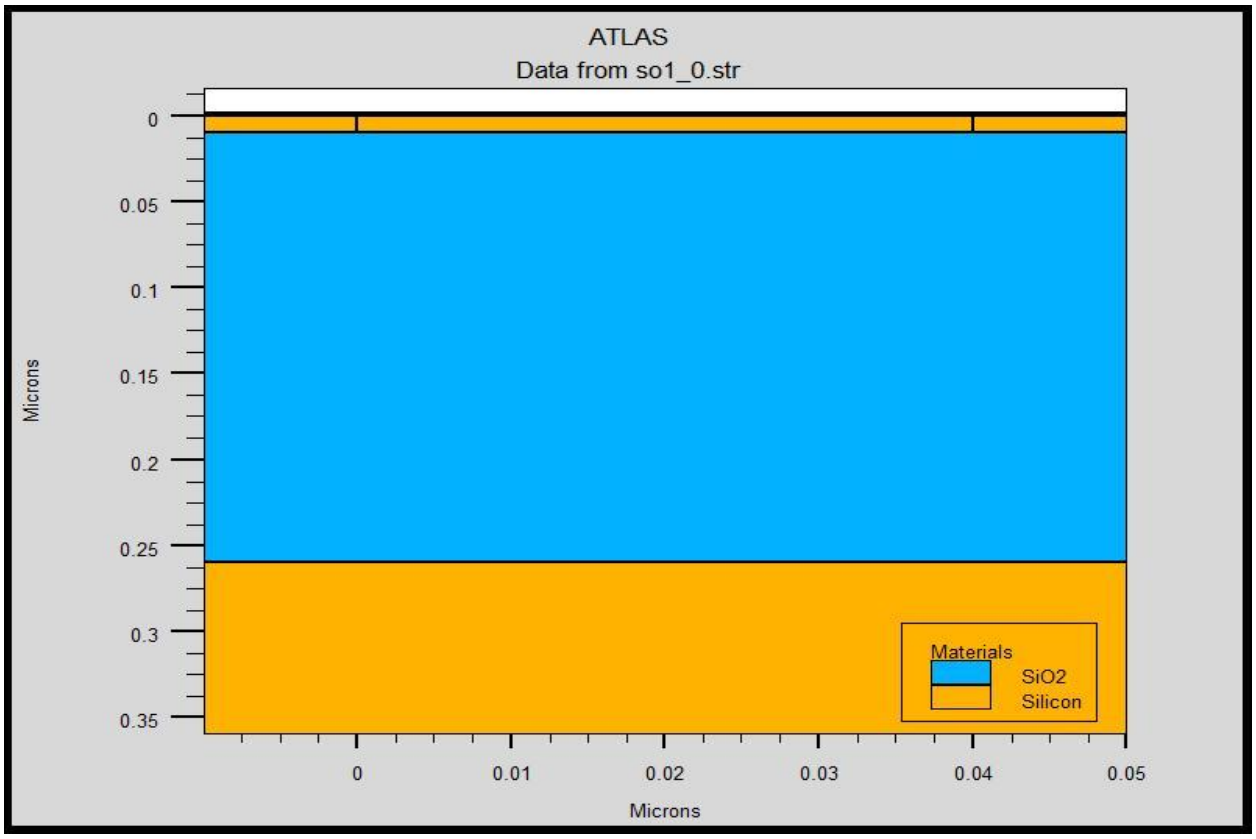
ANALYSIS:

It can be observed that in the graph the FET with drain voltage =0.5 V has low off-current as well as low on-current.

The FET with drain voltage = 1 V has more off-current and more on-current than the previous FET

The FET with drain voltage =1.5 V has same off-current as the previous one but has highest on-current.

DESIGN 3 : SIMULATED STRUCTURE OF TUNNEL FET FOR OUTPUT CHARACTERISTICS



Region 1-silicon dioxide layer has length of 2nm at the top of source, drain and gate
Region 2-gate region has length of length of 40 nm and width of 10 nm
Region 3- buried oxide or sio2 layer of has length of 60nm and width of 250nm
Region 4-substrate of si below insulator of has length of 60nm and width of 100nm
Region 5-source region has length of 10 nm and width of 10nm
Region 6-drain region has length of 10nm and width of 10 nm
Hence by dividing into specific regions, the structure was designed adequately. The box region is made up of sio2.and substrate is made up of silicon.
The doping concentration in region2---uniform, p-type $2x10^{17}$

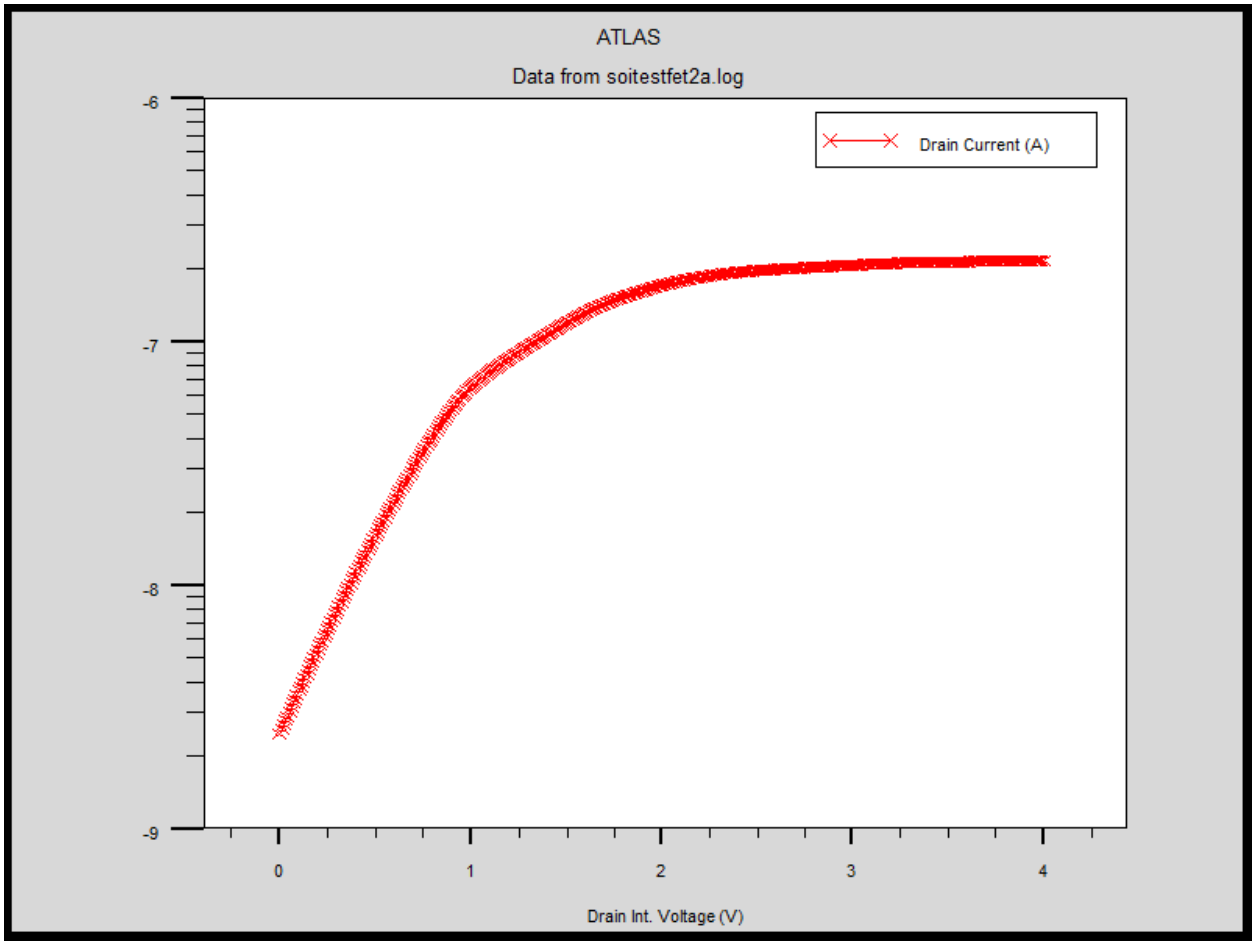
The doping concentration in region3---uniform, p-type $2x10^{17}$

The doping concentration in region5---uniform, n-type 10^{20}

The doping concentration in region6---uniform, n-type 10^{20}

OUTPUT CHARACTERISTICS

The Id vs Vds graph



Analysis:

The above curve was obtained by taking a constant gate voltage = 0.5 V . Different values of drain current was plotted against different values of drain voltage.

FUTURE SCOPE

Although the tunnel fet has lower OFF-current than the conventional MOSFET, both have relatively similar ON-current. So increasing the ON-current is a big challenge ahead. Certain methods are proposed like Double-Gate Silicon Tunnel FETs.

Semi-classical analytical models describing the two different tunneling parts in a TFETs: point tunneling and line tunneling will be improved as well as the BTBT modeling in indirect semiconductors such as grapheme which behaves as a direct semiconductor in TFETs.

The study of BTBT in indirect semiconductors will help demonstrate the impact of field-induced quantum confinement in TFET's.

CONCLUSION

In the above analysis we found that the electrical characteristics and performance of a TFET is better than a general MOSFET.As a possible successor to the MOSFET, it has a lower off-current than its predecessor. Due to low off-current the power dissipation is every low.

APPENDIX

1.SOFTWARE MODELLING OF TUNNEL-FET FOR CHECKING ENERGY BAND-LEVELS

```
go atlas
mesh space.mult=12.0
x.mesh loc=-0.030 spac=0.05
x.mesh loc=-0.0005001 spac=0.05
x.mesh loc=-0.0005 spac=0.0001
x.mesh loc=0.00 spac=0.0001
x.mesh loc=0.0005 spac=0.0001
x.mesh loc=0.0005001 spac=0.001
x.mesh loc=.0494999 spac=0.0001
x.mesh loc=.0495 spac=0.0001
x.mesh loc=.050 spac=0.0001
x.mesh loc=.0505 spac=0.0001
x.mesh loc=.0505001 spac=0.05
x.mesh loc=.080 spac=0.05

y.mesh loc=-.003 spac=0.01
y.mesh loc=-0.00001 spac=0.01
y.mesh loc=0.00 spac=0.0001
y.mesh loc=0.001 spac=0.0001
y.mesh loc=0.001001 spac=0.0001
y.mesh loc=.008999 spac=0.0001
y.mesh loc=.009 spac=0.0001
y.mesh loc=.010 spac=0.0001
y.mesh loc=.01001 spac=0.0001
```

```
region number=1  x.min=-0.030  x.max=0.00  y.min=-0.00  y.max=0.010  material=Silicon
region number=2  x.min=0.00  x.max=0.050  y.min=0.000  y.max=0.010  material=Silicon
region number=3  x.min=0.050  x.max=0.080  y.min=0.00  y.max=0.010 material=Silicon
region number=4  x.min=-0.030  x.max=0.080  y.min=-0.003  y.max=0.00   material=SiN
region number=5  x.min=-0.030  x.max=0.080  y.min=0.010  y.max=0.310   material=SiO2
region number=6  x.min=-0.030  x.max=0.080  y.min=0.310  y.max=0.560   material=Silicon


electrode name=source number=1  x.min=-0.030  x.max=-0.030  y.min=0.000  y.max=0.010
electrode name=drain number=2  x.min=0.080  x.max=0.080  y.min=0.000  y.max=0.010
electrode name=fgate number=3  x.min=0.000  x.max=0.050  y.min=-0.003  y.max=-0.003


electrode name=bgate number=4  x.min=-0.030  x.max=0.080  y.min=0.560 y.max=0.560


doping uniform conc=1e20 p.type direction=y region=1
doping uniform conc=1e17 p.type direction=y region=2
doping uniform conc=5e18 n.type direction=y region=3
doping uniform conc=1e18 p.type direction=y region=6

contact name=drain neutral
contact name=source neutral
contact name=fgate workfunction=4.5
contact name=bgate neutral




models temperature=300 srh fermi ni.fermi print \
 bbt.kl bgn

method   gummel newton itlimit=25 trap atrap=0.5 maxtrap=4 autonr nrcriterion=0.1 \
         tol.time=0.005 dt.min=1e-25
```

```
output band.temp traps  taurn taurp band.param con.band val.band \
qfn qfp


solve init
solve vdrain=0.1
solve vdrain=0.5
solve vdrain=0.5 outf= solve_vdrain0.5
solve vdrain=1 outf=solve_vdrain1
solve vdrain=1.5 outf=solve_vdrain1.5

load infile=solve_vdrain0.5
log outfile=mos_transfer0.5.log
solve vfgate=0 vstep=0.05 vfinal=2.4 name=fgate

tonyplot mos_transfer0.5.log

load infile=solve_vdrain1
log outfile=mos_transfer1.log
solve vfgate=0 vstep=0.05 vfinal=2.4 name=fgate

load infile=solve_vdrain1.5
log outfile=mos_transfer1.5.log
solve vfgate=0 vstep=0.05 vfinal=2.4 name=fgate

tonyplot mos_transfer1.5.log

save outf= soitestfet2a.str

tonyplot soitestfet2a.str

#extract name=" ss_soitestfet2a.log" 1.0/slope(maxslope(curve(v."fgate",log10(abs(i."drain")))))

#extract name="dydx2" deriv(v."fgate",i."drain",2) outfile="dydx2.dat"

#tonyplot dydx2.dat

tonyplot -overlay mos_transfer0.5.log mos_transfer1.log mos_transfer1.5.log

quit
```

2.SOFTWARE MODELLING FOR TUNNEL FET FOR TRANSFER CHARACTERISTICS

```
go atlas
mesh space.mult=8.0
x.mesh loc=-0.030 spac=0.05
x.mesh loc=-0.0005001 spac=0.05
x.mesh loc=-0.0005 spac=0.0001
x.mesh loc=0.00 spac=0.0001
x.mesh loc=0.0005 spac=0.0001
x.mesh loc=0.0005001 spac=0.001
x.mesh loc=.0494999 spac=0.0001
x.mesh loc=.0495 spac=0.0001
x.mesh loc=.050 spac=0.0001
x.mesh loc=.0505 spac=0.0001
x.mesh loc=.0505001 spac=0.05
x.mesh loc=.080 spac=0.05

y.mesh loc=-.003 spac=0.01
y.mesh loc=-0.0005 spac=0.0001
y.mesh loc=-0.00001 spac=0.0001
y.mesh loc=0.00 spac=0.0001
y.mesh loc=0.001 spac=0.0001
y.mesh loc=0.001001 spac=0.0001
y.mesh loc=.008999 spac=0.0001
y.mesh loc=.009 spac=0.0001
y.mesh loc=.010 spac=0.0001
```

```
y.mesh loc=.01001 spac=0.0001
y.mesh loc=.310 spac=0.0005
y.mesh loc=.500 spac=0.005


region number=1  x.min=-0.030  x.max=0.00  y.min=0.00  y.max=0.010  material=Silicon
region number=2  x.min=0.00  x.max=0.050  y.min=0.000  y.max=0.010  material=Silicon
region number=3  x.min=0.050  x.max=0.080  y.min=0.00  y.max=0.010 material=Silicon
region number=4  x.min=-0.030  x.max=0.080  y.min=-0.003  y.max=-0.0005   material=Si3N4
region number=5  x.min=-0.030  x.max=0.080  y.min=0.010  y.max=0.310   material=SiO2
region number=6  x.min=-0.030  x.max=0.080  y.min=0.310  y.max=0.500   material=Silicon
region number=7  x.min=-0.030  x.max=0.080  y.min=-0.0005  y.max=0.000  material=SiO2

electrode name=source number=1  x.min=-0.030  x.max=-0.030  y.min=0.000  y.max=0.010
electrode name=drain number=2  x.min=0.080  x.max=0.080  y.min=0.000  y.max=0.010
electrode name=fgate number=3  x.min=0.000  x.max=0.050  y.min=-0.003  y.max=-0.003
electrode name=bgate number=4  x.min=-0.030  x.max=0.080  y.min=0.500 y.max=0.500


doping uniform conc=1e20 p.type region=1
doping uniform conc=1e17 p.type region=2
doping uniform conc=5e18 n.type region=3
doping uniform conc=1e18 p.type region=6


 contact name=drain
 contact name=source
 contact name=fgate workfunction=4.5
 contact name=bgate

 mobility deln.cvt=1.65e13 delp.cvt=1.65e13

 models bbt.std bb.a=10e20 bb.b=10e7 bb.gamma=2.5 srh fldmob conmob consrh auger dglog bgn\
      b.electrons=2 b.holes=1 evsatmod=0 hvsatmod=0 cvt \
          boltzman print temperature=300

 method   gummel newton itlimit=25 trap atrap=0.5 maxtrap=4 autonr nrcriterion=0.1 \
          tol.time=0.005 dt.min=1e-25


 output band.temp traps  taurn taurp band.param con.band val.band \
 qfn qfp


 solve init
 solve qfactor=.001
 solve qfactor=.1
```

```
solve vdrain=0.1

solve vdrain=0.5 outf= solve_vdrain0.5
solve vdrain=1 outf=solve_vdrain1
solve vdrain=1.5 outf=solve_vdrain1.5

load infile=solve_vdrain0.5
log outfile=mos_transfer0.5.log
solve vfgate=0 vstep=0.01 vfinal=2.4 name=fgate

tonyplot mos_transfer0.5.log

load infile=solve_vdrain1
log outfile=mos_transfer1.log
solve vfgate=0 vstep=0.01 vfinal=2.4 name=fgate

tonyplot mos_transfer1.log

load infile=solve_vdrain1.5
log outfile=mos_transfer1.5.log
solve vfgate=0 vstep=0.01 vfinal=2.4 name=fgate

tonyplot mos_transfer1.5.log


save outf= soitestfet2a.str

tonyplot soitestfet2a.str

tonyplot -overlay mos_transfer0.5.log mos_transfer1.log mos_transfer1.5.log

quit
```

```
go atlas
mesh space.mult=8.0
x.mesh loc=-0.030 spac=0.05
x.mesh loc=-0.0005001 spac=0.05
x.mesh loc=-0.0005 spac=0.0001
x.mesh loc=0.00 spac=0.0001
x.mesh loc=0.0005 spac=0.0001
x.mesh loc=0.0005001 spac=0.001
x.mesh loc=.0494999 spac=0.0001
x.mesh loc=.0495 spac=0.0001
```

```
x.mesh loc=.0505 spac=0.0001
x.mesh loc=.0505001 spac=0.05
x.mesh loc=.080 spac=0.05

y.mesh loc=-.003 spac=0.01
y.mesh loc=-0.001 spac=0.0001
y.mesh loc=0.00 spac=0.0001
y.mesh loc=0.001 spac=0.0001
y.mesh loc=0.001001 spac=0.001
y.mesh loc=.008999 spac=0.001
y.mesh loc=.009 spac=0.0001
y.mesh loc=.010 spac=0.0001
y.mesh loc=.01001 spac=0.0001
y.mesh loc=.310 spac=0.001
y.mesh loc=.500 spac=0.001
```

```
region number=1  x.min=-0.030  x.max=0.00  y.min=0.00  y.max=0.010  material=Silicon
region number=2  x.min=0.00  x.max=0.050  y.min=0.000  y.max=0.010  material=Silicon
region number=3  x.min=0.050  x.max=0.080  y.min=0.00  y.max=0.010 material=Silicon
region number=4  x.min=-0.030  x.max=0.080  y.min=-0.003  y.max=0.00   material=SiO2
region number=5  x.min=-0.030  x.max=0.080  y.min=0.010  y.max=0.310   material=SiO2
region number=6  x.min=-0.030  x.max=0.080  y.min=0.310  y.max=0.500   material=Silicon
```

```
electrode name=source number=1  x.min=-0.030  x.max=-0.030  y.min=0.000  y.max=0.010
electrode name=drain number=2  x.min=0.080  x.max=0.080  y.min=0.000  y.max=0.010
electrode name=fgate number=3  x.min=0.000  x.max=0.050  y.min=-0.003  y.max=-0.003
electrode name=bgate number=4  x.min=-0.030  x.max=0.080  y.min=0.500 y.max=0.500


doping uniform conc=1e20 p.type region=1
doping uniform conc=1e17 p.type region=2
doping uniform conc=5e18 n.type region=3
doping uniform conc=1e18 p.type region=6

contact name=drain
contact name=source
contact name=fgate workfunction=4.5
contact name=bgate

mobility deln.cvt=1.65e13 delp.cvt=1.65e13

models bbt.std bb.a=10e20 bb.b=10e7 bb.gamma=2.5 srh fldmob conmob consrh auger dglog bgn\
     b.electrons=2 b.holes=1 evsatmod=0 hvsatmod=0 cvt \



        boltzman print temperature=300

method   gummel newton itlimit=25 trap atrap=0.5 maxtrap=4 autonr nrcriterion=0.1 \
        tol.time=0.005 dt.min=1e-25


output band.temp traps  taurn taurp band.param con.band val.band \
qfn qfp


solve init
solve qfactor=.001
solve qfactor=.1
solve qfactor=1
solve vfgate=0.1

solve vfgate=3

log outf=soitestfet2a.log

solve vdrain=0 vstep=0.01 vfinal=4 name=drain

tonyplot soitestfet2a.log
```

```
save outf= soitestfet2a.str

#extract name=" ss_soitestfet2a.log" 1.0/slope(maxslope(curve(v."fgate",log10(abs(i."drain")))))

tonyplot soitestfet2a.str
quit
```

REFERENCES

[1] W. Reddick and G. Amaratunga, "Silicon surface tunnel transistor," Appl. Phys. Lett., vol. 67, no. 4, 1995, pp. 494-496.

[2] 2006Kane EO. Theory of tunneling. J Appl Phys 1961;32:83

[3] Khatami Y, Banerjee K. Steep subthreshold slope n- and p-type tunnel-FET devices for low-power and energy-efficient digital circuits. IEEE TED 2009;56:2752

[4] R.Booth, M.White, H. wong and T. Krustick ."the effect of cahnnel impalnts on MOS transistor characterization" , IEEE Trans.Elec.Dev vol Ed-34, no12,1987,pp 2501-2509

[5] Atlas User's Manual by Silvaco International, May 26,

FIGURES

[1] M.j.Dort, J.W.Slotboo"Scaling of conventional Mosfet to the 0.1 micrometre regime" vol. 6 , Sept(1995)

[2] Cho, S., Kim, K.R., Park, B.-G., Kang, I.M.: RF performance and small-signal parameter extraction of junctionless silicon nanowire MOSFETs. IEEE Trans. Electron Devices **58**(5), 1388–1396(2011)

[3] Cho, S., Kim, K.R., Park, B.-G., Kang, I.M.: RF performance and small-signal parameter extraction of junctionless silicon nanowire MOSFETs. IEEE Trans. Electron Devices **58**(5), 1388–1396(2011)

[4] M.j.Dort, J.W.Slotboo"Scaling of conventional Mosfet to the 0.1 micrometre regime" vol. 6 , Sept(1995)

[5] K. Boucart and A.M.Ionesca "Threshold voltage in Tunnel Fets"

[6] Li Yu Chen, Zhou Chun yu "two dimensional threshold voltage model of nanoscale SOI TFET" vol 22, no 3 (2013)

[7] K. Boucart and A.M.Ionesca , "Double Gate Tunnel fet with high-K gate dielectric', IEEE Trans.Elec.Dev. vol 54,No 7,

[8] Kathy Boucart and Adrian Mihai Ionescu, IEEE Transactions on Electron Devices, VOL 54, NO 7, July 2007